	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	6	(signal adj override) and simulation and (processors or TTL) and enable and latch and disable	USPAT	2004/04/05 13:48
2	BRS	L2	3	(signal adj override) and (signal adj selection) and simulation and (processors or TTL) and enable and latch and disable	USPAT	2004/04/05 14:02
3	BRS	L6	941	simulation and ((digital adj device) or (HDL))	USPAT	2004/04/05 13:58
4	BRS	L7	1181	simulation and ((digital adj device) or (HDL))	USPAT	2004/04/05 13:58
5	BRS	L8	0	simulation and ((digital adj device) or (HDL)) and (signal adj override) and automated and (signal adj	USPAT	2004/04/05 14:01
6	BRS	L9	0	simulation and ((digital adj device) or (HDL)) and (signal adj override) and (signal adj selections)	USPAT	2004/04/05 14:01
7	BRS	L10	0	simulation and (HDL) and (signal adj override) and (signal adj	USPAT	2004/04/05 14:01
8	BRS	L11	804	simulation and (HDL)	USPAT	2004/04/05 14:01
9	BRS	L12	0	simulation and (HDL) and (signal adj override)	USPAT	2004/04/05 14:02
10	BRS	L13	900	signal adj override	USPAT	2004/04/05 14:02
11	BRS	L14	157	hardware adj simulators	USPAT	2004/04/05 14:04
12	BRS	L15	1	(hardware adj simulators) and (signal adj selection)	USPAT	2004/04/05 14:10
13	BRS	L16	0	(hardware adj simulators) and (signal adj selection) and override	USPAT	2004/04/05 14:09
14	BRS	L17	798	simulation and (hardware adj description adj language)	USPAT	2004/04/05 14:11
15	BRS	L18	10	simulation and (hardware adj description adj language) and (signal adj selection)	USPAT	2004/04/05 14:11
16	BRS	L19	0	simulation and (hardware adj description adj language) and (signal adj selection) and (signal adj override)	USPAT	2004/04/05 14:41
17	BRS	L20	0	simulation and (hardware adj description adj language) and (signal adj selection) and preclude	USPAT	2004/04/05 14:42

	Type	L #	Hits	Search Text	DBs	Time Stamp
18	BRS	L21	0	simulation and (hardware adj description adj language) and (signal adj selection) and (signal adj	USPAT	2004/04/05 14:42
19	BRS	L22	10	simulation and (hardware adj description adj language) and (signal adj selection)	USPAT	2004/04/05 15:05
20	BRS	L23	0	simulation and (hardware adj description adj language) and (signal adj selection) and (signal adj rejection)	USPAT	2004/04/05 14:43
21	BRS	L24	764	simulation and verilog	USPAT	2004/04/05 15:06
22	BRS	L25	50	simulation and verilog and override	USPAT	2004/04/05 15:06
23	BRS	L26	40	simulation and verilog and override and enable	USPAT	2004/04/05 15:18
24	BRS	L27	1	simulation and verilog and override and enable and (override near	USPAT	2004/04/05 15:20
25	BRS	L28	0	simulation and verilog and override and enable and (override near outputport)	USPAT	2004/04/05 15:20
26	BRS	L29	0	simulation and verilog and override and enable and (override near output) and latch	USPAT	2004/04/05 15:21
27	BRS	L30	14	simulation and verilog and override and enable and latch	USPAT	2004/04/05 15:30
28	BRS	L31	12	simulation and verilog and override and enable and latch and hierarchical	USPAT	2004/04/05 15:37
29	BRS	L32	12	simulation and verilog and override and enable and latch and hierarchical and storage	USPAT	2004/04/05 15:37